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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,152	02/06/2002	Sang-Eun Lee	8750-17	7500

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MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	3

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,152	LEE ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, marking are color-coded [claims 3, 8, and 13], demarcations [claim 7], marking have different shapes [claim 9], and a semiconductor defect inspection instrument [claim 10] must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-6, 8-9 and13 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, the claim recites "...marking defect locations on a wafer map..." The specification does not contain a full, clear and concise written description of what item(s) is used to mark the defect locations. For example, on page 6, lines 2-5, it states "...after the defect analysis is complete, a wafer map 10a is constructed using markings 100 to show the locations of the defects." However, no description is given of what item(s) is used for marking.

For examination purposes, the examiner is taking a position that any conventional marking device could be used to mark defects on the wafer. Since claims 2-6 depends off of claim 1, they are also rejected for the reason stated above.

Regarding claims 3, 8 and 13, the claims recite "...the dot marks are color-coded according to defect type and/or defect composition." The specification does not contain a full, clear and concise written description of color code used for defect type and/or defect composition. For example, on page 6, lines 5-6, it states "The marking, for instance, can be dot marks, with dot colors assigned depending on defect type..." However, no description is given of the colors for each defect type.

For examination purposes, the examiner is unable to conduct an adequate search on claims 3, 8 and 13 until further explanation is given.

Regarding claim 9, the claim recites "...the markings have different shapes depending on defect type." The specification does not contain a full, clear and concise written description of the different shapes used for the defect type. For example, on page 6, lines 5-6, it states "The marking, for instance, can be dot marks ...the marking can have different shapes depending on defect type." However, no description is given of the different shapes used for each defect type.

For examination purposes, the examiner is taking a position that any shape could be use for each defect type.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 4-7, 9-12, and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kinney et al (6122562).

Regarding claim 1, Kinney et al disclose a method of classifying defect chips [see Fig. 1], said method comprising: finding defect locations on a wafer (102) using a semiconductor defect inspection instrument(optical microscope 114) [see Abstract, lines 1-4 and column 3 lines 1-7]; analyzing the defect composition using the semiconductor defect inspection instrument (114) [see column 3 line 57-column 4 line 20]; and marking defect locations [via marking head 116] on a wafer map (102) using the same type of mark to identify of the same type of defect or defects containing similar compositions [see column 2 lines 1-13].

Regarding claim 2, Kinney et al disclose the marks on the wafer map (102) inherently are dot marks [see column 7 lines 31-34].

Regarding claim 4, Kinney et al disclose [see Fig. 5] graphing defect characteristics concurrently with marking defect locations on the wafer map(102) [see column 7 lines 48-65].

Regarding claim 5, Kinney et al disclose storing [via memory 148] and analyzing [CPU 146] defect characteristics electronically using software [see column 4 lines 48-67].

Regarding claim 6, Kinney et al disclose using the marks on the wafer map (102) to prepare graphs to assist in statistically analyzing the defects [see column 5 line 52- column 6 line 23].

Regarding claim 7, Kinney et al disclose [see Fig. 1] a wafer defect map (102), comprising: a schematic representation of a semiconductor wafer (102), including demarcations (position assemblies 118 and 119) corresponding to the location of chip boundaries; and a plurality of markings [not shown in the figure], each marking corresponding to a wafer defect, wherein locations of the markings on the wafer map (102) correspond to locations of the defects on the wafer, and wherein each marking is configured to identify a type of defect [see Abstract and column 2 lines 1-13].

Regarding claim 9, Kinney et al disclose the markings have different shapes depending on defect type [see column 4, lines 32-36 and lines 48-50 and column 7, lines 26-34].

Regarding claim 10, Kinney et al disclose the location and type of wafer defects is determined using a semiconductor defect inspection instrument (optical assembly 114) [see column 3 lines 1-8].

Regarding claim 11, Kinney et al disclose [see Fig. 1] a method of statistically analyzing defects on a semiconductor wafer (102), said method comprising: identifying [via optical assembly 114] a location and type of wafer defects [see Abstract, lines 1-4 and column 3 lines 1-7]; determining [via optical assembly 114] a composition of the wafer defects; preparing [via controller 140] a wafer defect map to visually represent the location and type of the wafer defects

[see column 5 lines 52-62]; and preparing [via controller 140] one or more charts and/or graphs to statistically represent defect characteristics [see Fig. 5 and column 5, line 52-column 6, line 23].

Regarding claim 12, Kinney et al disclose markings are placed on the wafer defect map (102) corresponding to defect locations [see Abstract and column 2 lines 1-13].

13. The method according to claim 12, wherein the markings are color-coded based on the type of defect represented thereby.

Regarding claim 14, Kinney et al disclose identifying a location and type of wafer defects comprises using an optical or scanning electron microscope (114) to identify the location and type of wafer defects [see column 3 lines 1-8].

Regarding claim 15, Kinney et al disclose determining a composition of the wafer defects comprises performing an AES analysis [via optical assembly 114] on the defects to determine the compositions thereof.

Regarding claim 16, Kinney et al disclose preparing [via controller 140] one or more charts and/or graphs comprises constructing a table comprising columns corresponding to defect type, defect composition, defect cause, and defect location [see Fig. 5 and column 5 lines 52-62 and column 7 lines 48-65].

Regarding claim 17, Kinney et al disclose preparing [via controller 140] one or more charts and/or graphs comprises preparing a bar graphs representing the number of defects according to defect type.

Regarding claim 18, Kinney et al disclose preparing [via controller 140] a wafer defect map to visually represent the location and type of the wafer defects, and preparing [via controller

140] one or more charts or graphs to statistically represent defect characteristics are performed electronically [via CPU 146].

Regarding claim 19, Kinney et al disclose identifying a location and type of wafer defects, and determining a composition of the wafer defects are also performed electronically [via CPU 146 in controller 140].

Regarding claim 20, Kinney et al disclose analyzing [via controller 140] the one or more charts or graphs to determine appropriate corrective action in a wafer fabrication process [see column 2 lines 1-45].

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wagner et al (5659172), Phan et al (5985497), Uritsky (6051845), Hennessey et al (6246787), Talbot et al (6252412), Simmons (6265232), Dotan (6407373) and Zeimantz (6441897) disclose a method and apparatus for analyzing defects on a wafer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
April 2, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800